

Garrett Kirsch

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EDUCATION

University of Pennsylvania, School of Engineering, Philadelphia, PA

May 2027

Candidate for BSE in Computer Engineering (GPA: 3.95)

Candidate for MSE in Electrical Engineering (GPA: 4.0)

Relevant Courses: Chip Design, Computer Architecture, OS, Embedded Systems, Digital IC, Analog IC, Machine Learning

PROFESSIONAL EXPERIENCE

CyberSavvy Lab | *Research Assistant*

May 2025 – November 2025

- Approached by Professor Jing Li to join her hardware security lab and work on cloud infrastructure.
- Worked closely with PhD student Linus Wong to create a local cluster and configure their FPGAs as cloud resources.
- Created a pipeline that allowed the team to more efficiently test their designs on available FPGAs.

Penn Engineering | *Teaching Assistant (Intro to Computer Systems)*

August – December 2024

- Helped to teach course that explored computers in different levels of abstraction: from transistors to C.
- Volunteered to hold an extra “conceptual” office hour for students who wanted to go deeper into the content.
- Led optional recitations for students, covering CMOS, digital logic, RISC-V, and C programming.

Microprocessor Performance Modeling | *Researcher, Prof. Benjamin Lee*

Jan 2025 – May 2025

- Conducted literature survey of chiplet-based and 3D microarchitectures, focusing on thermal and power implications.
- Performed some basic power roofline modeling to examine impact of different architectures.

Pieces for Developers | *Quality Assurance Intern*

May – August 2024

- Accepted to intern at a venture-backed start-up developing a breakthrough artificial memory technology.
- Tested pre-release builds of their desktop app and browser extensions during the launch of their Copilot feature.

Penn College Houses | *Residential Advisor*

August 2024 – present

- Built community across 20 residents with diverse backgrounds through creative programming and initiatives.

PROJECTS

Matrix Multiply Engine (mini-TPU)

- Designed a custom mini-TPU to perform matrix multiplication, loosely based off the original Google TPU architecture.
- Implemented 4x4 systolic array with custom memory schemes and I/O circuitry.
- Massive digital design with **over 70,000 transistors**, all done with manual layout and no standard cell libraries.

PennOS – Virtual Operating System

- Collaborated in a team of 4 to design a virtual operating system in C with its own filesystem, kernel, scheduler, and shell.
- Contributed heavily to the filesystem, implementing a FAT, Open File Table, and a File Descriptor Table for each process, as well as the kernel-level filesystem functions such as write, read, open, etc.

64-bit SRAM – [Link to Report](#)

- Designed and simulated an SRAM in Cadence, including the necessary peripheral circuits such as tristate buffers, row and column decoders, bit-line prechargers, and registers to hold inputs and outputs.
- Achieved reliable performance at 1 GHz clock operation.

Transimpedance Amplifier (TIA) – [Link to Report](#)

- Designed a single input, differential output TIA in Cadence to amplify signals from a photoresistor.
- Optimized and tested for gain, bandwidth, noise, power, and stable operation.

RISCV Processor

- Wrote a 32-bit RISC-V processor in Verilog over the course of a semester.
- Implemented a custom CLA and divider, pipelining, and a basic AXI4-Lite cache from the official Arm specifications.

Music to My Ears – An Embedded Systems Project

- Designed a music transposer that takes in a melody, shifts it a specified number of half-steps, and plays it back.
- Interfaced off-the-shelf keyboard with an Atmega328PB to drive transposed audio with a visual display for notes.

SKILLS

Coding Languages: Bash/Shell scripting, Verilog, CUDA, Java, JavaScript, OCaml, C, Assembly (RISC-V), Python

Platforms/Tools: Docker, Kubernetes, Spice, Cadence, Git, GitHub, Linux, Latex, Arduino, Hugo, Altium.

Hardware: Proficient with analog and digital IC design, linear circuit design, soldering, bare-metal C, PCB layout.